CLAIMS

1. A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source region spaced apart from each other toward opposite sides of the active area, a plurality of vertically stacked pairs of floating gates and control gates arranged in a row between the bit line diffusion and the source region, with the control gates being positioned above and aligned with the floating gates, a select gate and an erase gates aligned with and positioned on opposite sides of each of the stacked gates, with select gates at the ends of the row partially overlapping the bit line diffusion and the source region, a diffusion region in the active area beneath each of the erase gates, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion.

2. The memory cell array of Claim 1 wherein the control gates, the select gates and the erase gates surround the floating gates in a manner which provides a relatively large inter-gate capacitance for high-voltage coupling during an erase operation.

3. The memory cell array of Claim 1 wherein the control gates, the erase gates and the channel regions beneath the floating gates surround the floating gates in a manner which provides a relatively large capacitance for high-voltage coupling during a program operation.

4. The memory cell array of Claim 1 including a relatively thin tunnel oxide between the floating gates and the substrate, and relatively thick dielectrics between the floating gates and the other gates.

5. The memory cell array of Claim 4 wherein erase paths extend from the floating gates through the tunnel oxide to channel regions in the active area below, and high voltage is coupled to the floating gates from the control gates, the select gates and the erase gates.

6. The memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and high voltage is coupled to the floating gates from the control

gates, from the erase gates, and from the channel regions beneath the floating gates.

7. The memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and the select gate in a selected cell is biased at a lower voltage than the other select gates in the row to control channel current for efficient hot carrier injection during a program operation.

8. The memory cell array of Claim 1 wherein the erase gates are biased at a voltage near ground potential, and the select gates in unselected cells are biased at a relatively high voltage to turn on channels beneath them to form a conduction path between the bit line diffusion and the source region.

9. The memory cell array of Claim 1 wherein the bit line diffusion and source region are formed in a P-well, and an erase path is formed by a relatively high negative voltage on the control gates and a relatively low negative voltage on the select and erase gates, with the bit line diffusion and source region, and P-well at 0 volts.

10. The memory cell array of Claim 1 wherein the bit line diffusion and source region are formed in a P-well, and an erase path is formed by applying a relatively low positive voltage on the control gates, the select gates and the erase gates with the P-well at a relatively high positive voltage and the bit line and source diffusions floating.

11. The memory cell array of Claim 1 wherein a read path is formed by turning on the select transistors and the stacked control and floating gate transistors in unselected cells, with the common source at 0 volts, the bit line diffusion at 1 - 3 volts, the erase gates at a potential near zero volts, and the control gates for the unselected cells at a relatively high positive voltage, and the control gate of the selected cell is biased at 0 - 1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state.

12. The memory cell array of Claim 1 including an erase path which can erase all of the cells in the array simultaneously and a program path which is single cell selectable.

13. A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source region spaced from each other toward opposite sides of the active area, a plurality of control gates and floating gates stacked together and arranged in rows between the bit line diffusion and the source region, select gates and erase gates aligned with and positioned on opposite sides of the stacked gates, with select gates at both ends of each of the rows partially overlapping the bit line diffusion and the source region, diffusion regions in the active area beneath the erase gates, a bit line above each of the rows, and bit line contacts interconnecting the bit lines and the bit line diffusion.

14. The memory cell array of Claim 13 wherein the bit line for a row containing a selected cell to be programmed is held at 0 volts, a relatively low positive voltage is applied to the select gate for the selected cell, a relatively high positive voltage is applied to the common source, a relatively high positive voltage is applied to the control gate for the selected cell, a voltage near ground potential is applied to the erase gates, and a relatively high positive voltage is applied to the control gates for the unselected cells.

15. The memory cell array of Claim 13 wherein alternate ones of the cells are programmed by applying 0 volts to the bit line diffusion, a relatively positive voltage to the common source region, a relatively low positive voltage to the select gate for a selected cell, and a relatively high positive voltage to the control gate for the selected cell.

16. The memory cell array of Claim 13 wherein the bit line for a row containing a selected cell to be programmed is held at a relatively high positive voltage, a relatively low positive voltage is applied to a cell select gate for the selected cell, 0 volts is applied to the common source region, a relatively high positive voltage is applied to the control gate in the selected cell, a relatively high positive voltage is applied to the control gates of unselected cells, a voltage near ground potential is applied to the erase gates, and a relatively high positive voltage is applied to the control gates in the unselected cells.

17. The memory cell array of Claim 13 wherein alternate ones of the cells are programmed by applying 0 volts to the common source, a relatively positive voltage to the bit line diffusion, a relatively low positive voltage to the select gate for a selected cell, and a relatively high positive voltage to the control gate for the selected cell.

18. A NAND flash memory cell array, comprising: a substrate having an an active area, a bit line diffusion and a common source diffusion spaced apart from each other in the active area, a plurality of vertically stacked pairs of floating gates and control gates arranged in a row between the bit line and source diffusions, with the floating gates being relatively thin and the control gates being positioned above the floating gates, erase and select gates interposed between and aligned with the stacked gates, with select gates at the ends of the row partially overlying the bit line diffusion and the common source diffusion, relatively thin tunnel oxides between the side walls of the floating gates and adjacent ones of the select and erase gates, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion.

19. The memory cell array of Claim 18 including diffusion regions of N+ material in the active area beneath the erase gates.

20. The memory cell array of Claim 18 wherein the control gates are substantially thicker in vertical dimension and narrower in lateral dimension than the floating gates.

21. The memory cell array of Claim 18 including a relatively thin dielectric film between each of the floating gates and the substrate, and relatively thick dielectrics between the other gates and the substrate.

22. The memory cell array of Claim 18 wherein erase paths extend from the side walls of the floating gates through the tunnel oxides to adjacent ones of the erase and select gates, a relatively negative voltage is applied to the control gates, and a relatively positive voltage is applied to the erase and select gates, with high voltage coupling between the control gates and substrate and the floating gates, and electrons migrating from the floating gates to the select gates and erase gates.

23. The memory cell array of Claim 18 including a program path with a gate oxide between each of the floating gates and an underlying channel region in the substrate through which electrons can travel by tunneling to build up a negative charge on the floating gate.

24. The memory cell array of Claim 18 wherein a program path is formed between each of the floating gates and an underlying channel region in the substrate by applying a relatively negative voltage to the bit line diffusion and the substrate and a relatively positive voltage to the control gates so that electrons tunnel from the channel region to the floating gate and a negative charge builds up on the floating gate.

25. The memory cell array of Claim 18 wherein a program path is formed between bit line diffusion and a channel region in the substrate beneath the stacked gates in a selected cell by applying a relatively negative voltage to the bit line diffusion and substrate, a relatively positive voltage to the select gate for the cell, a relatively positive voltage to the control gate in the cell, and a voltage near ground potential to the erase gate for the cell.

26. The memory cell array of Claim 18 including a program path comprising a gate oxide between one the floating gates and an underlying channel region in the substrate through which electrons can travel by hot carrier injection to build up a negative charge on the floating gate.

27. The memory cell array of Claim 18 wherein a program path is formed between the floating gate in a selected one of the cells and an underlying channel region in the substrate by applying a voltage near ground potential to the common source diffusion, a relatively positive voltage to the bit line diffusion, a relatively low positive voltage to the select gate adjacent for the selected cell, and a relatively high positive voltage to the control gate in the cell so that electrons travel by hot carrier injection from the channel region to the floating gate and build up a negative charge on the floating gate.

28. The memory cell array of Claim 18 wherein alternate ones of the cells are programmed by applying a voltage near zero to the common source diffusion, a relatively positive voltage to the bit line diffusion, a relatively low voltage to the

select gate for the selected cell, and a relatively high voltage to the control gate in the cell.

29. The memory cell array of Claim 18 wherein a program path is formed between one the floating gates and an underlying channel region in the substrate by applying a voltage near ground potential to the bit line diffusion, a relatively positive voltage to the common source diffusion, a relatively low positive voltage to the select gate for the selected cell, and a relatively high positive voltage to the control gate in the cell so that electrons travel by hot carrier injection from the channel region to the floating gate and build up a negative charge on the floating gate.

30. The memory cell array of Claim 18 wherein alternate ones of the stacked are programmed by applying a voltage near zero to the bit line diffusion, a relatively positive voltage to the common source diffusion, a relatively low positive voltage to the select gate for the selected stacked cell, and a relatively high positive voltage to the control gate in the cell.

31. A process of fabricating a NAND flash memory cell array, comprising the steps of: forming an oxide layer on an active area in a silicon substrate, forming a first silicon layer on the oxide layer, forming a dielectric film on the first silicon layer, forming a second silicon layer on the dielectric film, etching away a portion of the second silicon layer to form a row of control gates with exposed side walls, forming an oxide on the side walls of the control gates, anisotropically etching away portions of the first silicon layer and the oxide layer beneath it using the oxide on the side walls of the control gates as a mask to form floating gates which are stacked beneath, self-aligned with and of greater lateral extent than the control gates, forming diffusions in the active area between the floating gates, forming a thermal oxide on the side walls of the floating gates and on the surface of the substrate between the floating gates, depositing a third silicon layer over the thermal oxide, removing portions of the third silicon layer to form erase and select gates between and self-aligned with the stacked control and floating gates, with select gates at two ends of the row, forming a bit line diffusion and a common source diffusion in the active area near the select gates at the ends of the rows, and forming a bit line above the row and a bit line contact which interconnects the bit line and the bit line diffusion.

32. A process of fabricating a NAND flash memory cell array, comprising the steps of: forming an oxide layer on an active area in a silicon substrate, forming a first silicon layer on the oxide layer, etching away portions of the first silicon layer to form silicon stripes which extend in a first direction above the active area, forming a first dielectric film on the silicon strips, forming a second silicon layer on the first dielectric film, forming a second dielectric film on the second silicon layer, etching away portions of the second dielectric film and the second silicon layer to form a row of control gates with exposed side walls, etching away portions of the first silicon layer and the first dielectric film to form floating gates which are stacked beneath and self-aligned with control gates, forming diffusions in the active area between the stacked gates, forming a third dielectric film on the side walls of the control and floating gates, depositing a third silicon layer over the third dielectric film, removing portions of the third silicon layer to form select gates and erase gates on opposite sides of the stacked gates, with select gates at both ends of each row, forming a bit line diffusion and a common source diffusion in the active area near the select gates at the ends of the rows, and forming bit lines above the rows and bit line contacts which interconnect the bit lines and the bit line diffusion.